Claims

WHAT IS CLAIMED IS:

1. ~~A USB host system comprising:~~

   a first processor implementing a function of a USB driver;

   a downstream USB port; and

   a communication area accessible both by a second processor and by the ~~first processor.~~

2. The USB host system in Claim 1 where the communication area is a dual port memory.

3. The USB host system in Claim 1 where the communication area consists of multiple FIFO registers.

4. The USB host system in Claim 1 where an interrupt polled from a USB interrupt pipe is converted to an interrupt signal to the Main Processor.

5. ~~The USB host system in Claim 1 where the said second processor interfaces the host system via a standard microprocessor bus.~~

6. The USB host system in Claim 1 where a hub is used to provide multiple downstream USB ports.

7. ~~The USB host system in Claim 1 where data in the communication area are directly sent out on the USB bus.~~

8. The USB host system in Claim 1 where data received from the USB bus are written directly in the communication area.

9. ~~The USB host system in Claim 1 where the said host system is used to provide~~ a USB host function to the said second processor.

10. The USB host system in Claim 1 where the said host system is used to provide a USB host function to the said second processor which runs an operating system supporting USB, by intercepting calls to the USBD in the said operating system.

11. A USB host system comprising:

    a first processor implementing a function managing a USB host controller;

    ~~a downstream USB port; and~~

~~an interface that provides a high-level USB pipe view of a USB system to a program running on a second processor.~~

12. The USB host system in Claim 11 where the said interface uses a memory that can be accessed by both the first processor and the second processor.

13. The USB host system in Claim 11 where the second processor interfaces the host system via a standard microprocessor bus.

14. The USB host system in Claim 11 where a hub is used to provide multiple downstream USB ports.

15. The USB host system in Claim 11 where the said host system is used to provide a USB host function to the said second processor.

16. The USB host system in Claim 1 where the said host system is used to provide a USB host function to the said second processor which runs an operating system supporting a USBD, and USB transfer request by the said second processor intercepting calls to the USBD in the said operating system.

17. An information processing system comprising:

a first processor; and

a data transfer host system comprising a second processor implementing a first data transfer driver managing a data transfer between the said first processor and a device; a data transfer port for connecting a device to the said data transfer host system; and an interface with the first processor that provides a high-level view of the data transfer process to the first processor.

18. The information processing system in Claim 17 where the said interface uses a memory area that can be accessed by both the said first processor and the said second processor.

19. The information processing system in Claim 17 where the said second processor is used to reduce the number of interrupts to the said first processor.

20. The information processing system in Claim 17 where the said second processor is used to reduce the frequency of interrupts to the said first processor.

21. The information processing system in Claim 17 where the said first processor interfaces the data transfer host system via a standard microprocessor bus.

22. The information processing system in Claim 17 where a hub is used to provide multiple ports for connecting a plural of devices.

23. The information processing system in Claim 17 where the said first processor contains a second data transfer driver capable of managing the same said data transfer and a data transfer request by the said first processor to the said second data transfer driver is carried out by the said data transfer host system.

24. ~~A USB host comprising:~~

a first processor implementing a function of a USB system;

a downstream USB port; and

a memory accessible by both the said first processor and an second processor external to the said USB host, whereby a first area of the memory with a first predetermined format is used for a first type of transfer, and a second area of the memory with a second predetermined ~~format is used for a second type of transfer.~~

25. The USB host in Claim 24 where a hub is connected to the downstream USB port so that multiple devices can be connected to the system.

26. The USB host in Claim 24 where the memory is connected to both the first processor and the second processor via a standard microprocessor bus interface.

27. The USB host in Claim 24 where a third area of the memory with a third predetermined format is used for reporting device connection, enumeration and removal to the second processor.

28. The third area of the storage device in Claim 27 where the said third area is in a part of the said memory which is read-only to the second processor.

29. The USB host in Claim 24 where a fourth area of the memory with a fourth predetermined format is used for sending a USB command to the said USB host.

30. The USB host in Claim 24 where the starting address of each memory area for

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a transfer is used to identify the transfer.

31. The USB host in Claim 24 where the second processor allocates the size of a memory area for a transfer to fit the need of the transfer.

32. The USB host in Claim 24 where the second processor allocates the number of the said areas to fit the need of a transfer.

33. The USB host in Claim 24 where the starting address of the said first area can be in different part of the memory.

34. The USB host in Claim 24 where the starting address of the said second area can be in different part of the memory.

35. The USB host in Claim 24 where the starting address of the said first and second area are in the same location of the memory.

36. The USB host in Claim 24 where the said predetermined formats of the said first and second areas are the same.

37. The USB host in Claim 24 where the starting address of the said first and second areas are stored at fixed locations of the memory.

38. The USB host in Claim 24 where the said second processor writes a transfer request in a said area in the memory and notifies the first processor with an interrupt signal.

39. The USB host in Claim 24 where the first processor writes the status or data of a transfer into a said area in the memory and notifies the said second processor with an interrupt signal.

40. The USB host in Claim 24 where a single format of the said second area implements isochronous, interrupt and bulk transfers.

41. A USB host comprising:

a first processor implementing a function of a USB system;

a downstream USB port; and

a memory accessible by both the said first processor and a second processor external to the said USB host, whereby the said second processor initiates a USB transfer by writing a transfer request, and data for the said transfer, if there is any, into a first area in the said memory,

and the said first processor carries out the transfer, and writes the status of the said transfer, and data from the said transfer, if there is any, into a second area in the said memory.

42. The USB host in Claim 41 where a hub is connected to the downstream USB port so that multiple devices can be connected to the system.

43. The USB host in Claim 41 where the memory is connected to both the first processor and the second processor via a standard microprocessor bus interface.

44. The USB host in Claim 41 where the said first area in the said memory and the said second area in the said memory are the same area.

45. The USB host in Claim 41 where the said first area in the said memory and the said second area in the said memory use a same predefined format.

46. The USB host in Claim 41 where the said second processor runs an operating system that supports USB and a USB transfer request by the said second processor to a USBD on the second processor is carried out by the said USB host.

47. The USB host in Claim 41 where when the said first processor carries out the transfer, and writes the status of the said transfer, and data from the said transfer, if there is any, into a second area in the said memory, the said USB host generates an interrupt signal to the said second processor to notify the said second processor.

48. The USB host in Claim 41 where when the said second processor initiates a USB transfer by writing a transfer request, and data for the said transfer, if there is any, into a first area in the said memory, the said second processor generates an interrupt signal to the said USB host to notify the said USB host.